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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/687,453	10/13/2000	James M. Van Dyke	18659-23	1345

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EXAMINER
CHEN, CHONGSHAN

ART UNIT	PAPER NUMBER
2172	

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No. 09/687,453	Applicant(s) VAN DYKE ET AL.	
	Examiner Chongshan Chen	Art Unit 2172	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 20 August 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☒ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *32-67*.

   Claim(s) withdrawn from consideration: *1-31*.

8. ☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

Continuation of 5. does NOT place the application in condition for allowance because: Applicant's arguments filed on 20 August 2003 regarding claims 32-67 have been fully considered but they are not persuasive.

As per applicant's arguments regarding claim 32 Kurihara does not disclose dividing graphics memory access bus into individual bus partitions have been considered but are not persuasive. Kurihara shows individual bus partitions of bus 3 (Fig. 1A) connect to plurality of graphic processors. Kurihara's invention provides a graphic data parallel processing apparatus having a plurality of graphic processors for simultaneously processing graphic data (Kurihara, col. 3, lines 10-15). If there is no individual bus partition dedicated to each graphic processor, data have to wait in turn before it can be transferred to each graphic processor, then the plurality of graphic processors won't be able to simultaneously process data. Therefore, in order to simultaneously process data, the system must have individual bus partitions connecting to its graphic processor for simultaneously transmitting data to the plurality of graphic processors.

As per applicant's arguments regarding claim 32 Kurihara does not address partitioned memory and routing data from said independently accessible memory partitions to said plurality of graphics processing unit via said individual bus partitions have been considered but are not persuasive. Kurihara shows independently accessible memory partitions (Fig. 1A, FIFO memories 5) connecting to plurality of graphics processors via individual bus partitions.

As per applicant's arguments regarding claim 34 Kurihara does not address mapping data to said independently accessible memory partitions in an interleaved fashion to balance memory load across independently accessible memory partitions have

been considered but are not persuasive. The examiner interprets interleave as mean transferring different sequence of data to different graphic processors. Kurihara teaches the graphic data controller, according to the type of the graphic data, selects one of the FIFO memories having sufficient space to receive the data (Kurihara, col. 4, lines 13-21). Kurihara's system will not transmit all data to a single FIFO memory while let other FIFO memories empty, it will balance the memory load by transferring data to different FIFO memories.

As per applicant's arguments regarding claim 37 Kurihara does not teach claimed arbiter circuits have been considered but are not persuasive. An arbiter is a functional module that accepts bus requests from requester module and grants control of data transfer bus to one requester at a time (see "IEEE 1000: The Authoritative Dictionary of IEEE Standards Terms", Seventh Edition, ISBN 0-7381-2601-2). Kurihara's invention has bus that transfers data between memory and graphic processors. Therefore, arbiters would have been included in Kurihara's system to grant control of the bus for transferring data.

As per applicant's arguments regarding claim 41 Kurihara does not address sub-set of said plurality of graphics processing units sharing a command and write data path have been considered but are not persuasive. Kurihara shows a single graphic data controller connecting to a plurality of graphic processors (Fig. 1A). Since there is only one graphic data controller, the read/write command would have shared a data path.

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